In the Claims:

Claims 1 to 26 stand of record in the case.

Claims 1, 5, 6, 13, 25 and 26 stand rejected.

Claims 2, 3, 4, 7-12 and 14-24 are objected to.

Explanation of Amendments in the Claims:

1.(currently amended) Apparatus for direct digital generation of a synthesized RF output signal at a desired output frequency comprising:

a high speed reference clock providing in an input signal having a series of signal reference edges at a frequency of the reference clock which is higher than the desired output frequency;

programmable digital delay elements arranged to receive the reference edges of the input reference clock and to generate delayed signal edges each at a calculated delay from a respective reference edge;

and a signal ~~combining~~ generating element for receiving the delayed signal edges and for generating the RF output signal therefrom;

wherein the signal generating element is arranged to directly generate the RF output signal so as to comprise a series of pulses each having a rising edge and a falling edge; and

wherein the signal generating element is arranged to generate the rising and a falling edges of the pulses at a digital timing determined by the delayed signal edges calculated from a respective reference edge.

2.(original) The apparatus according to Claim 1 wherein the programmable digital delay elements comprise high speed adders/accumulators wherein said adders/accumulators are arranged to determine the amount of delay implemented by the delay elements on the reference edge.

3.(original) The apparatus according to Claim 1 wherein the programmable digital delay elements comprise high speed adders/accumulators and a look-up table for providing increments to be added to calculate said delay.

4.(original) The apparatus according to Claim 3 wherein the lookup table has a multiple set of lookup tables to be used for temperature compensation of the programmable delay line.

5.(currently amended) The apparatus according to Claim 1 wherein ~~the reference clock provides an external input with high frequency absolute accuracy and very low phase noise performance~~ the signal generating element is arranged to generate both the rising and a falling edges of the pulses from rising edges only of the reference edges of the input signal of the reference clock.

6 .(currently amended) The apparatus according to Claim 1 wherein ~~the programmable digital delay elements are arranged such that said reference edge may be either the rising or falling edge of the reference clock~~ the signal generating element is arranged to generate both the rising and a falling edges of the pulses from falling edges only of the reference edges of the input signal of the reference clock.

7.(original) The apparatus according to Claim 1 wherein said programmable digital delay elements have separate controls for producing the rising and falling edges of the output from the same input edge of the reference clock.

8.(original) The apparatus according to Claim 1 wherein the programmable digital delay elements are arranged to be varied by altering the input clock signal.

9.(original) The apparatus according to Claim 2 wherein in association

with the high speed adders/accumulators of the programmable delay elements there is provided a pulse swallow circuit which is controlled by the carry bits (overflow bits) of the high speed adders/accumulators in order to extend the delay to multi cycles of the input reference clock.

10.(original) The apparatus according to Claim 9 wherein the pulse swallow circuit is arranged to discard multiple reference clock pulses.

11.(original) The apparatus according to Claim 9 wherein said pulse swallow circuit is located prior to or following the programmable delay element.

12.(original) The apparatus according to Claim 1 wherein the programmable digital delay elements are arranged such that 360 degrees of phase delay of the programmable delay is calibrated to 2^n of the phase accumulator value using a look up table or microprocessor.

13.(currently amended) The apparatus according to Claim 1 wherein the signal ~~combining~~ generating element comprises a flipflop.

14 .(currently amended) The apparatus according to Claim ~~13~~ 1 wherein said ~~flipflop~~ the signal generating element is arranged to ~~combine~~ generate both the separate rising and falling ~~edge~~ edges of the pulses ~~delays~~ so as to form any desired duty cycle of the RF output signal.

15 .(currently amended) The apparatus according to Claim 14 wherein said signal generating element is arranged to generate both the separate rising and falling edges of the pulses such that said ~~output~~ duty cycle of the RF output signal is not dependent on an input duty cycle of the input signal.

16 .(currently amended) The apparatus according to Claim 14 wherein

said duty cycle of the RF output signal can be varied by changing the difference in initialization values of the programmable digital delay elements ~~for the rising and falling edge delay control~~.

17 .(currently amended) The apparatus according to Claim 16 wherein said ~~increment values~~ calculated delay for the rising and falling edges are the same value.

18.(original) The apparatus according to Claim 2 wherein the worst case frequency resolution is determined by the equation in which the reference frequency is divided by 2^n, where n is equal to the number of bits in the high speed adders/accumulators.

19.(original) The apparatus according to Claim 2 wherein the high speed adders/accumulators are arranged such that increasing the number of bits in the adder math increases the frequency resolution with negligible degradation in the phase noise performance.

20.(original) The apparatus according to Claim 2 wherein the high speed adders/accumulators are arranged such that the number of bits of math used in the adder can be equal to or exceed the number of bits of control in lookup table and /or the programmable delay.

21.(original) The apparatus according to Claim 2 wherein the high speed adders/accumulators are arranged such that the speed can be increased using parallel processing in the adders, and/or accumulators.

22.(original) The apparatus according to Claim 1 wherein the programmable digital delay elements include a lookup table wherein all the answers of

the pattern are pre-computed and stored.

23.(currently amended) The apparatus according to Claim 2 wherein the output frequency is set from ~~an increment~~ a delay value according to the following equation:

~~Increment~~ Delay Value = $((f_{ref} / f_{out}) - 1) * 2^n$

where f_{ref} = Reference clock (103) frequency

f_{out} = Output (110) frequency

n = Number of bits in the accumulator math.

24.(currently amended) The apparatus according to Claim 2 wherein the signal generating element is arranged to generate both the separate rising and falling edges of the pulses so as to form any desired duty cycle of the RF output signal and wherein the duty cycle is set by initializing the difference of the initializing values of the two accumulators according to the following equation:

The reference clock frequency divided by the desired output frequency multiplied by $2^{\wedge n}$ multiplied by (p/100), where p is the percentage duty cycle and n is the number of bits in the accumulator math.

25.(cancelled)

26.(cancelled)